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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,588	08/18/2003	Kitrick Sheets	1376.720US1	4010

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,588	SHEETS, KITRICK	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are presented for examination in this application (10,643,588) filed on August 18, 2003.

Duty To Disclose Information Material To Patentability

2. The following is a quotation of the appropriate paragraphs of 37 C.F.R. 1.56 that recites Applicants' duty to disclose information material to patentability:

"Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by § § 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Schimmel (US 6,105,113).

As to claim 1, Schimmel discloses **a method for translating a virtual memory address into a physical memory address** [System and Method for maintaining Translation Lookaside Buffer (TLB) Consistency (title)] **in a multi-node system** [figure 3 shows a multi-node system], **the method comprising**:

providing the virtual memory address at a source node [when a CPU requires a physical memory address that is associated with a virtual memory address (column 4, lines 8-13)];

determining that a translation for the virtual memory address does not exist [figure 9, step 916];

determining a physical node to query based on the virtual memory address [when a CPU requires a translation, CPU or an operating system searches TLB. If the translation is not found in TLB (i.e., a TLB "miss"), the desired translation is loaded from the page tables in memory by hardware, software, firmware, or any combination thereof (column 9, lines 20-29); figure 5];

querying an emulated remote translation table (ERTT) segment on the physical node for the translation for the virtual memory address [figures 5-8 show the page tables and translation tables to facilitate translations of a virtual address into a physical address]; **and**

if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node [figure 9 shows the steps of obtaining the desired translation from the beginning to the end, including step 928, send PTE to processor, and step 930, place PTE, VM address tag and PTE address tag in TLB].

As to claim 2, Schimmel teaches that **the ERTT segment resides in a generally accessible memory on the physical node** [figures 5-8 show the page tables and translation tables to facilitate translations of a virtual address into a physical address; these tables are stored in the main memory or cache (figure 8), which are distributed among and shared by all the nodes (figure 3), hence they are generally accessible on the physical node (column 7, lines 1-7)].

As to claim 3, Schimmel teaches that **determining a physical node includes mapping a virtual node to the physical node** [figures 5-8 show the mapping between virtual entities and physical entities].

As to claim 4, Schimmel teaches that **mapping a virtual node to a physical node uses a mapping provided by an ERTT header located at a well-known location to all nodes used by an application** [figures 5-8 show the page tables and translation tables to facilitate the mapping between virtual entities and physical entities,

figure 9 shows the steps of accomplishing the mapping; abstract; column 7, lines 50-67; column 8].

As to claim 5, Schimmel teaches that **the ERTT header is located on a predetermined virtual node** [figures 5-8 show the page tables and translation tables to facilitate translations of a virtual address into a physical address; these tables are stored in the main memory or cache (figure 8), which are distributed among and shared by all the nodes (figure 3). Since none of the node has all the translation information needed by itself, the collection of all the memories appears to be a predetermined virtual node as far as each of the node is concerned].

As to claim 6, Schimmel discloses a computerized system for managing virtual address translations, the system comprising:

a plurality of nodes [figure 3 shows a multi-node system] **available for executing programs** [figures 9-10 show the computer programs], **each of said nodes having a node memory** [figure 3 shows the main memory and cache memory]; **and**

an operating system [when an operating system changes a PTE ... (abstract)]

executable by a source node of the plurality of nodes, the operating system operable to:

receive a virtual memory address at the source node [when a CPU requires a translation, CPU or an operating system searches TLB];

determine that a translation for the virtual memory address does not exist on the source node [figure 9, step 916];

determine a physical node to query based on the virtual memory address [when a CPU requires a translation, CPU or an operating system searches TLB. If the translation is not found in TLB (i.e., a TLB "miss"), the desired translation is loaded from the page tables in memory by hardware, software, firmware, or any combination thereof (column 9, lines 20-29); figure 5];

query an emulated remote translation table (ERTT) segment on the physical node for the translation for the virtual memory address [figures 5-8 show the page tables and translation tables to facilitate translations of a virtual address into a physical address]; **and**

if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node [figure 9 shows the steps of obtaining the desired translation from the beginning to the end, including step 928, send PTE to processor, and step 930, place PTE, VM address tag and PTE address tag in TLB].

As to claim 7, refer to "As to claim 2."

As to claim 8, refer to "As to claim 3."

As to claim 9, refer to "As to claim 4."

As to claim 10, refer to "As to claim 5."

As to claim 11, refer to "As to claim 1" and "As to claim 6."

As to claim 12, refer to "As to claim 2."

As to claim 13, refer to "As to claim 3."

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Scott (US Patent Application Publication 2004/0044872).

As to claim 1, Scott discloses **a method for translating a virtual memory address into a physical memory address** [Remote Translation Mechanism for a Multi-Node System (title)] **in a multi-node system** [figure 1 shows a multi-node system], **the method comprising**:

providing the virtual memory address at a source node [abstract];

determining that a translation for the virtual memory address does not exist [abstract; figure 4; paragraph 0006];

determining a physical node to query based on the virtual memory address [figure 4];

querying an emulated remote translation table (ERTT) segment on the physical node for the translation for the virtual memory address [the corresponding ERTT is the Global Address Space identifier (GASID) and the Remote Translation Table (RTT) as described in paragraph 0019]; **and**

if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node [figure 4; paragraph 0019].

As to claim 2, Scott teaches that **the ERTT segment resides in a generally accessible memory on the physical node** [paragraph 0019].

As to claim 3, Scott teaches that **determining a physical node includes mapping a virtual node to the physical node** [figures 2-3 and 5 show the mapping between virtual entities and physical entities].

As to claim 4, Scott teaches that **mapping a virtual node to a physical node uses a mapping provided by an ERTT header located at a well-known location to all nodes used by an application** [abstract; figure 5 shows where the ERTT is located with respect to the source node].

As to claim 5, Scott teaches that **the ERTT header is located on a predetermined virtual node** [figure 5 shows where the ERTT is located with respect to the source node. Since none of the node has all the translation information needed by itself, the collection of all the memories appears to be a predetermined virtual node as far as each of the node is concerned].

As to claim 6, Scott discloses a computerized system for managing virtual address translations, the system comprising:

a plurality of nodes [figure 1 shows a multi-node system] **available for executing programs** [figure 4 shows the computer programs], **each of said nodes having a node memory** [figure 1]; **and**

an operating system [it is common knowledge that all computers and processors are equipped with an operating system] **executable by a source node of the plurality of nodes, the operating system operable to**:

receive a virtual memory address at the source node [abstract];

determine that a translation for the virtual memory address does not exist on the source node [abstract; figure 4; paragraph 0006];

determine a physical node to query based on the virtual memory address [figures 2-3 and 5 show the mapping between virtual entities and physical entities];

query an emulated remote translation table (ERTT) segment on the physical node for the translation for the virtual memory address [abstract; figure 5 shows where the ERTT is located with respect to the source node]; **and**

if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node [figure 4; paragraph 0019].

As to claim 7, refer to "As to claim 2."

As to claim 8, refer to "As to claim 3."

As to claim 9, refer to "As to claim 4."

As to claim 10, refer to "As to claim 5."

As to claim 11, refer to "As to claim 1" and "As to claim 6."

As to claim 12, refer to "As to claim 2."

As to claim 13, refer to "As to claim 3."

As to claim 14, refer to "As to claim 4."

As to claim 15, refer to "As to claim 5."

7. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Scott et al. (US 6,925,547), "Remote Address Translation in a Multiprocessor System."
- Deneau, (US 6,684,305), "Multiprocessor System Implementing Virtual Memory Using a Shared Memory, and a Page Replacement Method for Maintaining Paged memory Coherence."
- Frank et al., (US 6,490,671), "System for Efficiently Maintaining Translation Lookaside Buffer Consistency in a Multi-Threaded, Multi-Processor Virtual Memory System."
- Hansen, (US 6,101,590), "Virtual Memory System with Local and Global Virtual Address Translation."

Conclusion

8. Claims 1-15 are rejected as explained above.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

August 19, 2005

PIERRE BATAILLE
PRIMARY EXAMINER

8/25/05